Docket No.: 42390.P7299

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

In re the application of:	)	
	)	
Cline, Leslie E.	)	
	)	
Serial No.: 09/540,676	)	Examiner: Lee, C. E.
	)	
Filed: 03/31/2000	)	Art Unit: 2189
	)	
For: METHOD AND APPARATUS FOR LOGICAL DETACH FOR A HOT-PLUG-IN DATABUS	)	

APPELLANT'S BRIEF UNDER 37 CFR § 1.192
IN SUPPORT OF APPELLANT'S APPEAL TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Hon. Commissioner for Patents
Mail Stop Appeal Brief – Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant hereby submits this Brief in triplicate in support of an appeal from a final decision of the Examiner, in the above-referenced case. Appellant respectfully requests consideration of this appeal by the Board of Patent Appeals and Interference for allowance of the above-referenced patent application.

TABLE OF CONTENTS

I. Real Party in Interest

The real party in interest in the present appeal is Intel Corporation, a Delaware Corporation headquartered in Santa Clara, California, the assignee of the present application.

II. Related Appeals and Interferences

There are no related appeals or interferences to appellant's knowledge that would have a bearing on any decision of the Board of Patent Appeals and Interferences.

III. Status of the Claims

Claims 2, 6, 16, and 22 are cancelled.

Claims 1, 3 through 5, 7 through 15, and 17 through 21 are pending in the application.

Claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 stand rejected under 35 U.S.C. §103(a) as being anticipated by Huang, et al., U.S. patent number 6,131,134 (hereinafter *Huang*), in view of Rafferty et al., U.S. patent number 6,141,719 (hereinafter *Rafferty*) and Pollard, et al., U.S. patent number 5,754,870 (hereinafter *Pollard*). Claim 12 stands rejected under 35 U.S.C. §103(a) as being anticipated by *Huang*, in view of *Rafferty* and *Pollard* as applied to claims 1, 3 through 5, 7 through 11,

15, and 17 through 21 above and further in view of Decuir, U.S. patent number 5,781,028 (hereinafter *Decuir*). Claims 13 and 14 stand rejected under 35 U.S.C. §103(a) as being anticipated by *Huang*, in view of *Rafferty* and *Pollard* as applied to claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 above and further in view of Takasu, Japanese patent number JP 407058800 A (hereinafter *Takasu*).

Claims 1, 3 through 5, 7 through 15, and 17 through 21 are the claims presently under this appeal.

IV. Status of Amendments

Appellants have not submitted any amendments after the Final Office Action mailed on 04/15/2004.

V. Summary of the Invention

Appellant's disclosure describes a method and apparatus for logically detaching a hot-plug-in data bus (such as a Universal Serial Bus or IEEE 1394) without the need for physically detaching the bus.

In one embodiment, shown in Figure 5 of the application, the disclosure describes how a pull-up resistor 546, coupled to a serial data bus wire (USB D+) 524 at the near end of the bus 530, may be switched on or off by a detach control signal (HPWR) 516 sent from the far end of the bus to a switch (pull-up control) 544. The circuit 540 containing the pull-up resistor 546 and switch 544 may become logically detached from the bus when the switch 544 is off.

When the circuit 540 wishes to become logically connected to the bus 530 again, it may send a wake-up signal (WAK#) 554 to the far end of the bus, where it may cause the detach control signal 516 to close switch 544 and activate pull-up resistor 546. This may cause circuit 540 to become logically connected to the bus.

The specification of the present application, page 10, line 16, through page 13, line 5 describes the above Figure 5 embodiment.

VI. Issues

1. Whether claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 are unpatentable under 35 U.S.C. §103(a) over Huang, et al., U.S. patent number 6,131,134 (hereinafter *Huang*), in view of Rafferty et al., U.S. patent number 6,141,719 (hereinafter *Rafferty*) and Pollard, et al., U.S. patent number 5,754,870 (hereinafter *Pollard*).

2. Whether claim 12 is unpatentable under 35 U.S.C. §103(a) over *Huang*, in view of *Rafferty* and *Pollard* as applied to claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 above and further in view of Decuir, U.S. patent number 5,781,028 (hereinafter *Decuir*).

3. Whether claims 13 and 14 are unpatentable under 35 U.S.C. §103(a) over by *Huang*, in view of *Rafferty* and *Pollard* as applied to claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 above and further in view of Takasu, Japanese patent number JP 407058800 A (hereinafter *Takasu*).

VII. Grouping of Claims (Independent Claims **Bolded**)

With regards issue 1, claims **1**, 3 through 5, 7, **8** through 11, **15**, 17, 18, **19** through 21 are under appeal.

With regards issue 2, claim 12 is under appeal.

With regards issue 3, claims 13 and 14 are under appeal.

VIII. Argument

A. Claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 Are Not Obvious In View of *Huang*, *Rafferty* and *Pollard*.

Claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 stand rejected under 35 U.S.C. §103(a) over Huang, et al., U.S. patent number 6,131,134 (hereinafter *Huang*), in view of Rafferty et al., U.S. patent number 6,141,719 (hereinafter *Rafferty*) and Pollard, et al., U.S. patent number 5,754,870 (hereinafter *Pollard*).

To establish a *prima facie* case of obviousness, case law as cited in the MPEP requires three criteria.

> First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure.

In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991), cited in MPEP section 706.02(j).

Moreover, the Federal Circuit has recently cautioned that the Patent Office must support its rejections for reasons that are stated on

the record that establish why a particular combination would have been motivated by the prior art. It is inadequate to just state in conclusory fashion that just because two elements existed in the prior art, that someone should have or would have been motivated to combine them. A specific teaching or a specific principle must be stated that makes the combination obvious.

> The need for specificity pervades this authority. See, e.g., In re Kotzab, 217 F.3d 1365, 1371, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000) ("particular findings must be made as to the reason the skilled artisan, with no knowledge of the claimed invention, would have selected these components for combination in the manner claimed"); In re Rouffet, 149 F.3d 1350, 1359, 47 USPQ2d 1453, 1459 (Fed. Cir. 1998) ("even when the level of skill in the art is high, the Board must identify specifically the principle, known to one of ordinary skill, that suggests the claimed combination. In other words, the Board must explain the reasons one of ordinary skill in the art would have been motivated to select the references and to combine them to render the claimed invention obvious."); In re Fritch, 972 F.2d 1260, 1265, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (the examiner can satisfy the burden of showing obviousness of the combination "only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references").

In re Sang Su Lee, 277 F.3d 1338, 61 USPQ 1430 (Fed. Cir. 2002).

Appellant submits that (a) no specific showing of motivation to combine the references has been provided, and (b) that the references, even if combined, do not provide the claimed invention.

a. No Specific Showing of Motivation to Combine

The contention in the Final Office Action that it would be obvious to combine *Huang*, *Rafferty* and *Pollard* is both factually and legally erroneous.

i. Factually, *Huang*, *Rafferty* and *Pollard* Do Not Suggest Motivation to Combine

Huang teaches logically disconnecting a USB databus, but only under local control by the databus node containing the pull-up resistor. Nothing in *Huang* teaches any control for logically disconnecting coming from the far side of the databus.

Rafferty teaches a switch for connecting numerous USB upstream and downstream modules via a switching system incorporating a central bus. A pair of switches is shown to connect the pull-up resistor to either the high-speed data line D+ or the low-speed data line D-. The control lines for these switches are NOT sourced from the opposite end of a USB databus but rather from the internals of the switching system.

Even if *Rafferty* taught the control lines for his switches being sourced from the opposite end of a USB databus, which he does not, there is nothing in the facts of *Huang* and *Rafferty* which would suggest combining them. They each solve very different problems by switching in

and out the pull-up resistor: *Huang* does it for logical disconnect purposes and *Rafferty* does it to select the speed of the interface. Therefore there is nothing in the facts of *Huang* and *Rafferty* that would intrinsically lead someone of skill in the art to combine them.

Pollard teaches a power control signal going to a switch on a plug-in card to turn the power on or off to a power-consuming module on the plug-in card. *Pollard* does NOT teach any such signals going over any serial databus. All these items in *Pollard* are on the *same side* of the *only* disclosed serial link (item 72, Pollard Figure 2). Any serial databus in *Pollard* is incidental to the invention of *Pollard*, so there is nothing in the facts of *Pollard* that would intrinsically lead someone of skill in the art to combine the power control of *Pollard* with the serial databus techniques of *Huang* and *Rafferty*.

The entirety of the explanation from the Final Office Action of why *Rafferty* should be combined to the apparatus of *Huang* reads as follows:

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a serial bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e. logically attaching and detaching) of said apparatus (i.e. USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

Final Office Action dated 04/15/2004, paragraph 3 (in 4 places).

The Office Action makes no explanation whatsoever as to why the "advantage of simulating insertion and removal" is suggested in either *Rafferty* or *Huang*. Hence there is no intrinsic teaching that such an "advantage" would be useful.

The entirety of the explanation from the Final Office Action of why Pollard should be combined to the apparatus of Huang and Rafferty reads as follows:

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said wake-up signal wire, as disclosed by Pollard, in said apparatus, as disclosed by Huang, as modified by Rafferty, so as said switch (i.e., power connect switch) to operate responsive to said wake-up signal (i.e., status signal) indicating the operability of said near end of said data bus (i.e., a status monitor indicative of the operability of the remote data link capability) from said near end (i.e., power-consuming elements on the card) to said far end (i.e., power source in the computer), which is disclosed at Pollard, col. 2, lines 43-48.

Final Office Action dated 04/15/2004, paragraph 3 (in 4 places).

The Office Action makes no explanation whatsoever as to why the advantage "to have included said wake-up signal wire" is suggested in either *Pollard*, *Rafferty*, or *Huang*. Hence there is no intrinsic teaching that such an inclusion would be useful.

ii. Legally, Burden Not Met

Furthermore, appellant submits that the evidentiary burden for an obviousness rejection has not been met. The Federal Circuit was specific in its admonitions in *In re Sang Su Lee*, quoted above. Particular factual findings are required to underpin a section 103 rejection. The Final Office Action must explain the *reasons* one of ordinary skill in the art would have been *motivated* to select the references and to combine them. Here, the Final Office Action only makes the following conclusory statements.

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have received a logically detaching control signal from a far end of a serial bus, as disclosed by Rafferty, in said apparatus, as disclosed by Huang, for the advantage of simulating insertion and removal (i.e. logically attaching and detaching) of said apparatus (i.e. USB device) by a corresponding far end device (i.e., a corresponding peripheral device; See Rafferty, col. 1, lines 50-58).

> Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said wake-up signal wire, as disclosed by Pollard, in said apparatus, as disclosed by Huang, as modified by Rafferty, so as said switch (i.e., power connect switch) to operate responsive to said wake-up signal (i.e., status signal) indicating the operability of said near end of said data bus (i.e., a status monitor indicative of the operability of the remote data link capability) from said near end (i.e.,

power-consuming elements on the card) to said far end (i.e., power source in the computer), which is disclosed at Pollard, col. 2, lines 43-48.

Final Office Action dated 04/15/2004, paragraph 3 (in 4 places).

No factual basis is given as to why someone would be *motivated* to combine the *Pollard*, *Rafferty*, and *Huang* references. Only by using the *hindsight subject to the present application* would one of ordinary skill examine the *Pollard*, *Rafferty*, and *Huang* references. And as shown in section (b) immediately following, these three references even when combined do not teach the invention claimed in claims 1, 3 through 5, 7 through 11, 15, and 17 through 21.

b. Even If Combined, *Huang*, *Rafferty*, And *Pollard* Do Not Meet The Claim Limitations

As discussed above, appellant submits that insufficient *motivation* exists to combine the *Huang*, *Rafferty*, and *Pollard* references. Even assuming, however, that such a combination is made, the combination itself does not include all of the elements and limitations of appellant's claims.

In the Final Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang, as modified by Rafferty, does not teach influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said

data bus from said near end of said data bus to said far end of said data bus." The Office Action then claims that *Pollard* discloses these claim limitations. Appellant wishes to point out that *Pollard* presents a set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of *parallel* data bus may be *inferred* due to the characterization of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

Independent claim 1 recites in pertinent part "a *serial* data bus." (Appellant's emphasis added.) This recitation in the method of claim 1 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, appellant therefore believes that amended independent claim 1 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Independent claim 1 further recites in pertinent part "controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus *from a far end of* ***said*** *serial data bus* to cause an apparatus containing said

first resistor and said switch to enter a logically detached state." (Appellant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

Rafferty Figure 4 is a detail of Figure 3, but Figure 4 has been confusingly presented geometrically reversed left-to-right. In order to more easily discuss the subject matter of *Rafferty*, appellant has prepared a sketch (attached as Appendix B of the present brief) that combines Figures 3 and 4 with the details of Figure 4 shown in geometric order consistent with Figure 3.

The sketch shows a resistor Rpu and a pair of switches 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of serial data bus (A). *Rafferty* states at column 3, lines 24 to

28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Appellant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Appellant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14*. As the claim recites "said serial data bus", the controlling signal must come from the far end of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a *different* data bus. Appellant therefore submits that the element of claim 1 under discussion is not taught by *Rafferty*.

Appellant therefore believes that independent claim 1 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 3 through 5, and 7, depend from independent claim 1, and because appellant believes that independent claim 1 is now allowable, appellant further believes that claims 3 through 5, and 7, are now allowable.

In the Final Office Action at paragraph 3, in reference to claim 8, it was admitted that "Huang, as modified by Rafferty, does not teach a wake-up signal wire separate from said data transmission wires of said data bus to send a wake-up signal from said near end of said data bus to said far end of said data bus to influence said detach control signal." The Office Action then claims that *Pollard* discloses these claim limitations. Appellant again wishes to point out that *Pollard* presents a set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of *parallel* data bus may be *inferred* due to the characterization of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

Independent claim 8 recites in pertinent part "a *serial* data bus." (Appellant's emphasis added.) This recitation in the apparatus of claim 8 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data

busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, appellant therefore believes that amended independent claim 8 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Independent claim 8 further recites in pertinent part "a detach control signal wire separate from data transmission wires of a serial data bus coupled to said switch at a near end of said serial data bus, to receive *a detach control signal sent from a far end of* ***said*** *serial data bus* to cause said apparatus to enter a logically detached state." (Appellant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 8, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

The sketch attached as Appendix B of the present brief, as discussed previously, shows a resistor Rpu and a pair of switches 24, 26

coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of serial data bus (A). *Rafferty* states at column 3, lines 24 to 28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Appellant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Appellant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14*. As the claim recites "*said* serial data bus", the controlling signal must come from the far end of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a

different data bus. Appellant therefore submits that the element of claim 8 under discussion is not taught by *Rafferty*.

Appellant therefore believes that independent claim 8 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 9 through 15, and 17, depend from independent claim 8, and because appellant believes that independent claim 8 is now allowable, appellant further believes that claims 9 through 15, and 17, are now allowable.

In the Office Action at paragraph 3, in reference to claim 15, it was admitted that "Huang, as modified by Rafferty, does not teach means for influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said data bus from said near end of said data bus to said far end of said data bus." The Office Action then claims that *Pollard* discloses these claim limitations. Appellant again wishes to point out that *Pollard* presents a set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of *parallel* data bus may be *inferred* due to the characterization of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

Independent claim 15 recites in pertinent part "a *serial* data bus."

(Appellant's emphasis added.) This recitation in the apparatus of claim 15 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, appellant therefore believes that amended independent claim 15 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Independent claim 15 further recites in pertinent part "means for controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus *from a far end of said serial data bus* to cause said apparatus to enter a logically detached state." (Appellant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a

serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

The sketch attached as Appendix B of the present brief, as discussed previously, shows a resistor Rpu and a pair of switches 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of serial data bus (A). *Rafferty* states at column 3, lines 24 to 28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Appellant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Appellant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16 does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14*. As the claim recites "said serial data bus", the controlling signal must come from the far end

of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a *different* data bus. Appellant therefore submits that the element of claim 15 under discussion is not taught by *Rafferty*.

Appellant therefore believes that independent claim 15 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 16 through 21 depend from independent claim 15, and because appellant believes that independent claim 15 is now allowable, appellant further believes that claims 16 through 21 are now allowable.

In the Final Office Action at paragraph 3, in reference to claim 19, it was admitted that "Huang, as modified by Rafferty, does not teach a wake-up control signal separate from said data transmission wires of said data bus to send a wake-up signal from said near end of said data bus to said far end of said data bus; and said second circuit to send said detach control signal responsive to said wake-up signal." The Final Office Action then claims that *Pollard* discloses these claim limitations. Appellant again wishes to point out that *Pollard* presents a set of mating *connectors* 26, 28 and does not expressly teach *any* data bus between the host computer 22 and the plug-in card 30. At the most some sort of

parallel data bus may be *inferred* due to the characterization of connectors 26, 28 as "preferably a standard 68-pin connector" (*Pollard* column 4 lines 17 through 22).

Independent claim 19 recites in pertinent part "a *serial* data bus." (Appellant's emphasis added.) This recitation in the system of claim 19 is supported in the specification on page 1, line 18 through page 2 line 2, identifying both the Universal Serial Bus data bus of Figures 1 through 6 and the IEEE-1394 data bus of Figures 7 through 9 as serial data busses. As the Final Office Action has admitted that the limitations cited above are not found in *Huang* or *Rafferty*, and as there is no support for such a limitation with respect to a *serial* data bus disclosed in *Pollard*, appellant therefore believes that amended independent claim 19 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Independent claim 19 further recites in pertinent part "a detach control signal wire separate from data transmission wires of said serial data bus coupled to said switch to receive a detach control signal sent from *said far end of said serial data bus* to said near end of said serial data bus." (Appellant's emphasis added.) In the Office Action at paragraph 3, in reference to claim 1, it was admitted that "Huang does not teach said logically detaching control signal (e.g. switch controlling signal for simulating removal of USB device) sent from a far end of said serial data bus." The Office Action then states that "Rafferty discloses a

USB selector switch, wherein a logically detaching control signal (e.g., switch controlling signal for simulating removal of USB device; See Fig. 4 and col. 3, lines 13 - 29) is sent from a far end (i.e. from a corresponding peripheral module: See col. 3, lines 26 – 28) of a serial data bus (i.e. bus 14 of Fig. 3; See col. 2., lines 43 – 45)."

The sketch attached as Appendix B of the present brief, as discussed previously, shows a resistor Rpu and a pair of switches 24, 26 coupled to a near end of serial data bus (A), whose corresponding far side is in "downstream USB device 22". The switches have control signals "LS select" and "HS select". However, these control signals are *not* sent from the far side of serial data bus (A). *Rafferty* states at column 3, lines 24 to 28, that "the switches 24, 26 are controlled by data supplied from a corresponding peripheral module 12 based on the respective peripheral device 20 connected to the peripheral module 12 and by direction from the controller 18." *Rafferty* continues at column 3, lines 41 – 44, that "once the switch 10 is ready for operation, the switches 24, 26 are operated in accordance with the peripheral module 12, if any, that is communicating with the downstream module 16." Appellant has shown the controlling signal (data) from the peripheral module 12 to the switches 24, 26 as dashed lines E and F.

Appellant submits that the controlling signal coming from peripheral module 12 to the switches 24, 26 of downstream module 16

does *not* come from the far end of serial data bus (A) between downstream module 16 and downstream USB device 22, but rather instead *from the far end of a second data bus 14*. As the claim recites "said serial data bus", the controlling signal must come from the far end of the *same* serial data bus that is coupled to the resistor and switch. In the case of *Rafferty*, it does not. The resistor and switch are coupled to the near end of one serial data bus: the controlling signal comes from a *different* data bus. Appellant therefore submits that the element of claim 19 under discussion is not taught by *Rafferty*.

Appellant therefore believes that amended independent claim 19 is allowable over the cited *Huang*, *Rafferty*, and *Pollard* references.

Because claims 20 and 21 depend from independent claim 19, and because appellant believes that independent claim 19 is now allowable, appellant further believes that claims 20 and 21 are now allowable.

Appellant respectfully submits that all the claim elements and limitations of claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 are not disclosed in the combined *Huang*, *Rafferty*, and *Pollard* references. Therefore appellant submits that a proper *prima facie* case of obviousness has not been made out in the Office Action mailed 04/15/2004. Appellant therefore submits that claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 are patentable over the combined

Huang, *Rafferty*, and *Pollard* references.

B. Claim 12 Is Not Obvious In View Of *Huang*, *Rafferty*, *Pollard*, and *Decuir*.

Claim 12 stands rejected under 35 U.S.C. §103(a) over *Huang*, in view of *Rafferty* and *Pollard* as applied to claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 above and further in view of Decuir, U.S. patent number 5,781,028 (hereinafter *Decuir*).

Claim 12 depends from independent claim 8. As appellant has shown that independent claim 8 is patentable over the cited references, dependent claim 12 must also be patentable over the cited references. Appellant therefore believes the argument made in paragraph 4 of the Final Office Action mailed 04/15/2004 is moot, and that claim 12 is patentable over the combined *Huang*, *Rafferty*, *Pollard*, and *Decuir* references.

C. Claims 13 And 14 Are Not Obvious In View Of *Huang*, *Rafferty*, *Pollard*, and *Takasu*.

Claims 13 and 14 stand rejected under 35 U.S.C. §103(a) over *Huang*, in view of *Rafferty* and *Pollard* as applied to claims 1, 3 through 5, 7 through 11, 15, and 17 through 21 above and further in view of Takasu, Japanese patent number JP 407058800 A (hereinafter *Takasu*).

Claims 13 and 14 depend from independent claim 8. As appellant has shown that independent claim 8 is patentable over the cited references, dependent claims 13 and 14 must also be patentable over the cited references. Appellant therefore believes the argument made in paragraph 5 of the Final Office Action mailed 04/15/2004 is moot, and that claims 143 and 14 are patentable over the combined *Huang*, *Rafferty*, *Pollard*, and *Takasu* references.

Conclusion

Appellant respectfully submits that all claims now pending are in condition for allowance. Such action is earnestly solicited at the earliest possible date. If there is a deficiency in fees, please charge our Deposit Acct. No. 02-2666.

Respectfully submitted,

Date: 30 June 2004

Dennis A. Nicholls, Reg. No. 42,036

12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8598

IX. Appendix A: Claims Involved in Appeal (Clean Copy)

Presented below is a complete listing of claims.

1. (Previously presented) A method, comprising:

providing a first resistor with a first end and a second end, said first end coupled to a switch and said second end coupled to a serial data bus wire at a near end of a serial data bus;

controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus from a far end of said serial data bus to cause an apparatus containing said first resistor and said switch to enter a logically detached state;

influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said serial data bus from said near end of said serial data bus to said far end of said serial data bus; and

switching a biasing voltage from said resistor utilizing said switch.

2. (Canceled)

3. (Original) The method of claim 1, wherein said first resistor is configured as a pull-up resistor.

4. (Original) The method of claim 3, further comprising detecting said switching of said biasing voltage.

5. (Original) The method of claim 4, further comprising determining a logically detached state responsive to said detecting.

6. (Canceled)

7. (Previously presented) The method of claim 1, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

8. (Previously presented) An apparatus, comprising:

a first resistor with a first end and a second end;

a switch coupled to said first end of said first resistor and to a bias voltage;

a detach control signal wire separate from data transmission wires of a serial data bus coupled to said switch at a near end of said serial data bus, to receive a detach control signal sent from a far end of said serial data bus to cause said apparatus to enter a logically detached state;

a wake-up signal wire separate from said data transmission wires of said serial data bus to send a wake-up signal from said near end of said serial data bus to said far end of said serial data bus to influence said detach control signal; and

a serial data bus wire of said serial data bus coupled to said second end of said first resistor.

9. (Previously presented) The apparatus of claim 8, wherein said switch may apply said bias voltage to said first end of said first resistor responsively to said detach control signal on said detach control signal wire.

10. (Previously presented) The apparatus of claim 9, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

11. (Previously presented) The apparatus of claim 8, wherein said serial data bus carries universal serial bus data.

12. (Previously presented) The apparatus of claim 8, wherein said serial data bus carries IEEE-1394 bus data.

13. (Previously presented) The apparatus of claim 8, further comprising a second resistor with a first end and a second end, said first end coupled to said serial data bus wire.

14. (Previously presented) The apparatus of claim 13, wherein said second end of said second resistor is coupled to signal ground.

15. (Previously presented) An apparatus, comprising:

means for providing a first resistor with a first end and a second end, said first end coupled to a switch and said second end coupled to a serial data bus wire at a near end of a serial data bus;

means for controlling said switch with a detach control signal sent on a detach control signal wire separate from data transmission wires of said serial data bus from a far end of said serial data bus to cause said apparatus to enter a logically detached state;

means for influencing said detach control signal with a wake-up signal sent on a wake-up signal wire separate from said data transmission wires of said serial data bus from said near end of said serial data bus to said far end of said serial data bus; and

means for switching a biasing voltage from said resistor utilizing said switch.

16. (Canceled)

17. (Previously presented) The apparatus of claim 15, further comprising means for detecting said switching of said biasing voltage.

18. (Previously presented) The apparatus of claim 15, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

19. (Previously presented) A system, comprising:

a serial data bus with a near end and a far end;

a first circuit, coupled to said near end, including a first resistor with a first end and a second end, a switch coupled to said first end of said first resistor and to a bias voltage, a serial data bus wire of said data bus coupled to said second end of said first resistor, a detach control signal wire separate from data transmission wires of said serial data bus coupled to said switch to receive a detach control signal sent from said far end of said serial data bus to said near end of said serial data bus, and a wake-up control signal wire separate from said data transmission wires of said serial data bus to send a wake-up signal from said near end of said serial data bus to said far end of said serial data bus; and

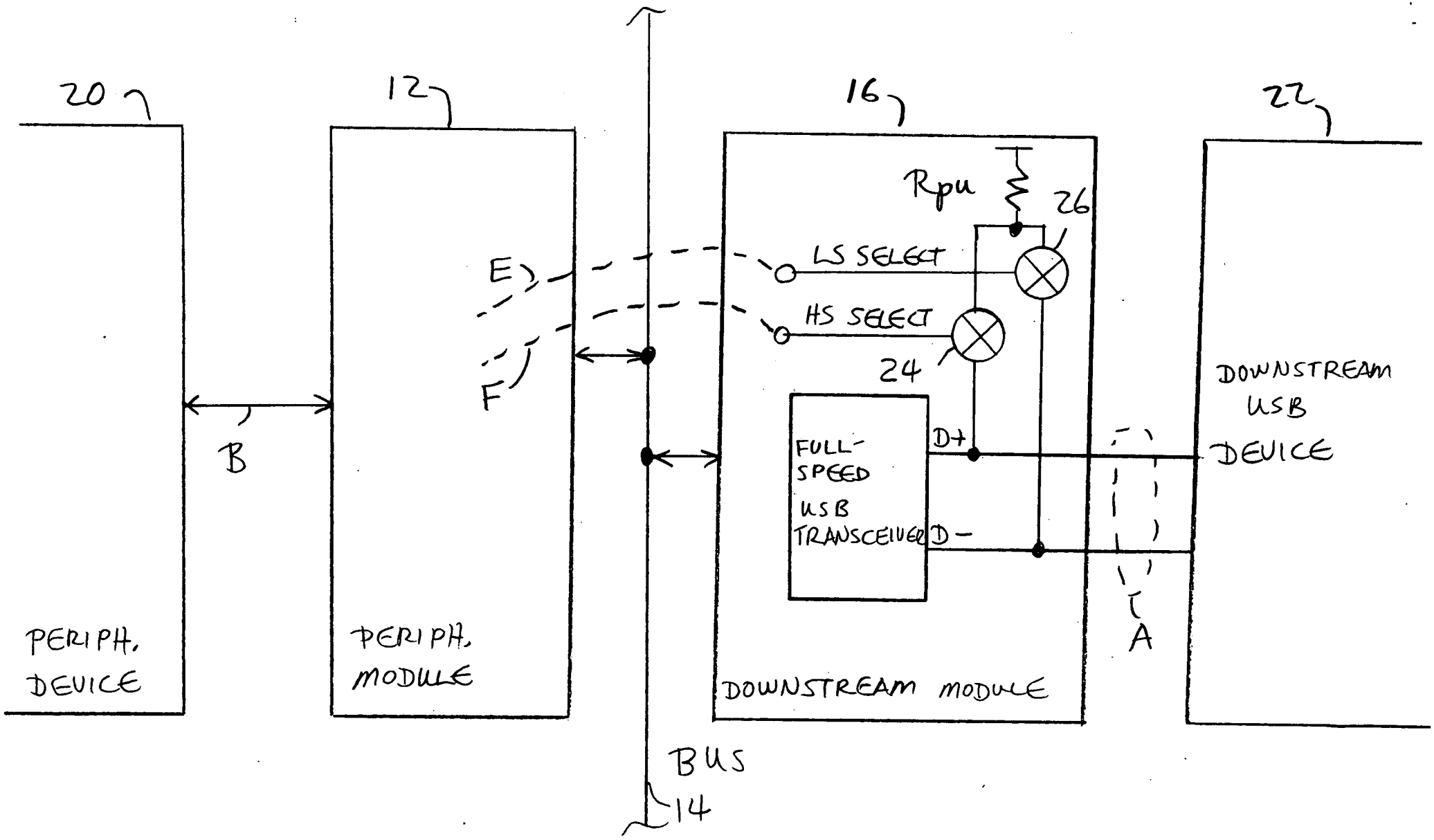
a second circuit, coupled to said far end, to send said detach control signal responsive to said wake-up signal to cause said first circuit to enter a logically detached state.

20. (Previously presented) The system of claim 19, wherein said switch may apply said bias voltage to said first end of said first resistor responsively to said detach control signal.

21. (Previously presented) The system of claim 19, wherein said detach control signal is asserted when said wake-up signal is de-asserted.

22. (Canceled)

X. Appendix B: Sketch Combining Figures 3 and 4 Of Rafferty, et. al, U.S. Patent No. 6,141,719



COMBINED FIGS. 3+4
US PAT #. 6,141,719 "RAFFERTY"

FIRST CLASS CERTIFICATE OF MAILING
(37 C.F.R. § 1.8(a))

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

on June 30, 2004.
Date of Deposit

Anne Collette
Name of Person Mailing Correspondence

Anne Collette — 6/30/2004
Signature — Date